WHAT IS CLAIMED IS:

1. A data processor comprising:

an instruction execution pipeline comprising:

a read stage;

a write stage; and

a first execution stage comprising E execution units capable of producing data results from data operands;

a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by said write stage of said instruction pipeline via at least one of W write ports of said register file; and

bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage.

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2. The data processor as set forth in Claim 1 wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage.

3. The data processor as set forth in Claim 2 further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage.

4. The data processor as set forth in Claim 3 further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage.

5. The data processor as set forth in Claim 4 further comprising a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage.

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6. The data processor as set forth in Claim 5 further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage.

7. The data processor as set forth in Claim 6 wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer.

8. The data processor as set forth in Claim 7 wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer.

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9. The data processor as set forth in Claim 8 wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer.

10. The data processor as set forth in Claim 9 wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer.

11. A processing system comprising:

a data processor;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, wherein said data processor comprises:

an instruction execution pipeline comprising:

a read stage;

a write stage; and

a first execution stage comprising E execution units capable of producing data results from data operands;

a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by said write stage of said instruction pipeline via at least one of W write ports of said register file; and

bypass circuitry capable of receiving data results from output channels of source devices in at least one of said

write stage and said first execution stage, said bypass circuitry comprising a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage.

12. The processing system as set forth in Claim 11 wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage.

13. The processing system as set forth in Claim 12 further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage.

14. The processing system as set forth in Claim 13 further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage.

15. The processing system as set forth in Claim 14 further comprising a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage.

16. The processing system as set forth in Claim 15 further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage.

17. The processing system as set forth in Claim 16 wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer.

18. The processing system as set forth in Claim 17 wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer.

19. The processing system as set forth in Claim 18 wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer.

20. The processing system as set forth in Claim 19 wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer.